CLAIMS:

1. (Currently Amended) A write controller for controlling memory storage operation of an Elastic Buffer, comprising:

a comparator mechanism which detects if link data from a source contains an IDLE signal;

a Jabber counter mechanism which counts each cycle of a link clock in which an IDLE signal is not detected, and resets said count each time said IDLE signal is detected, and which asserts a DISABLE signal for a single link clock cycle if said count reaches a programmed time-out value; and

a logic gate which logically combines outputs from said comparator mechanism and said Jabber counter mechanism to generate a Write control signal for prohibiting a corresponding link data sequence from being stored in said memory storage of said Elastic Buffer so as to prevent data overflow in said memory storage;

wherein said memory storage corresponds to one of a first-in, first-out (FIFO) register and a succession of D-type flip-flops having an elasticity required to synchronize said link data to a receiver clock subsequently used to retrieve said link data from said memory storage as receiver data; and

wherein said memory storage comprises a plurality of addressable memory locations determined by the potential differences in frequencies of the link clock and the receiver clock, and non-IDLE characters included in said link data.

2. (Original) The write controller as claimed in claim 1, wherein said comparator mechanism comprises:

a first comparator which determines if received link data contains a first IDLE sequence of said IDLE signal; and

a second comparator which determines if the received link data contains a second IDLE sequence of said IDLE signal.

3. (Original) The write controller as claimed in claim 1, wherein said Jabber counter mechanism comprises:

a N-bit counter which counts each cycle of said link clock in which an IDLE signal is not detected, and resets said count each time said IDLE signal is detected and said DISABLE signal is asserted for a single link clock cycle if said count reaches said programmed time-out value;

an OR gate which logically combines outputs from said comparator mechanism and said DISABLE signal to reset said count of said N-bit counter; and

a N-bit equality comparator which compares said count of said N-bit counter with said programmed time-out value and asserts said DISABLE signal if said count reaches said programmed time-out value.

4. (Original) The write controller as claimed in claim 1, wherein said comparator mechanism corresponds to two equality comparators, and said logic gate corresponds to an NOR gate.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) The write controller as claimed in claim 1 ~~6~~, further comprising operation at a link clock for selecting as a write address the address of a memory location of said memory storage to store said link data therein, and for preventing an IDLE signal included in said link data from being stored in said memory storage so as to prohibit data overflow in said memory storage.

8. (Original) The write controller as claimed in claim 7, further comprising a write pointer which operates at said link clock for selecting as said write address the address of a memory location of said memory storage to store said link data therein.

9. (Original) The write controller as claimed in claim 8, wherein said write pointer comprises a gray code counter.

10. (Original) The write controller as claimed in claim 7, wherein said Elastic Buffer further comprises a read control mechanism which operates at a receiver clock for selecting as a read address the address of a memory location of said memory storage to retrieve said link data as receiver data, and for inserting No-Operation (NOP) sequences into said receiver data when said memory storage is determined empty so as to prohibit data underflow in said memory.

11. (Original) The write controller as claimed in claim 10, wherein said read control mechanism comprises:

a read pointer which operates at said receiver clock for selecting as said read address the address of a memory location of said memory storage to retrieve said link data as said receiver data in dependence upon whether said memory storage is determined empty;

an output controller which determines said memory storage as empty when said read address corresponds to said write address; and

an output selector which inserts said No-Operation (NOP) sequences into said receiver data when said memory storage is determined empty.

12. (Original) The write controller as claimed in claim 11, further comprising a synchronizer which synchronizes the current value of said write address in a link clock domain with the current value of said read address in a receiver clock domain.

13. (Original) The write controller as claimed in claim 9, wherein said link data is received from said source via physical links in compliance with the Next Generation I/O (NGIO) Link Architecture Specification.

14. (Original) The write controller as claimed in claim 11, wherein said output controller comprises:

a plurality of XNOR gates each of which logically combines said read address and said write address in synchronous with said read address; and

an AND gate which logically combines logic outputs from the XNOR gates and produces an output signal indicating whether said memory storage is empty.

15. (Original) The write controller as claimed in claim 11, wherein said read pointer comprises a gray code counter.

16. (Original) The write controller as claimed in claim 11, wherein said output selector comprises a multiplexer for selecting between said receiver data and said NOP sequences inserted in said receiver data in dependence upon whether said memory storage is determined empty.

17. (Currently Amended) A computer network, comprising:

a host system;

at least one remote system;

a multi-stage switch comprising a plurality of different switches which interconnect said host system via a host channel adapter to said remote system via a remote channel adapter along different physical links for data communications, and

at least an elastic buffer provided in said host channel adapter of said host system for transferring data from a physical link into said host channel adapter which, said elastic buffer comprising:

a memory storage coupled to receive link data from said physical link and to store said link data in a plurality of addressable memory locations;

a write control mechanism which operates at a link clock for selecting as a write address the address of a memory location of said memory storage to store said link data, said write control mechanism comprising a Jabber counter which counts against a programmed time-out value to prevent a corresponding link data sequence from being stored in said memory storage so as to prohibit data overflow in said memory storage; and

a read control mechanism which operates at a receiver clock for selecting as a read address the address of a memory location of said memory storage to retrieve said link data as receiver data, and for inserting No-Operation (NOP) sequences into said receiver data when said memory storage is determined empty so as to prohibit data underflow in said memory storage;

wherein said write control mechanism further comprises:

a write controller which operates at said link clock for prohibiting said IDLE signal included in said link data from being stored in said memory storage; and

a write pointer which operates at said link clock for selecting as said write address the address of a memory location of said memory storage to store said link data therein.

18. (Canceled)

19. (Currently Amended) The computer network as claimed in claim 17 ~~18~~, wherein said write controller comprises:

a first comparator which determines if received link data contains a first IDLE sequence of said IDLE signal;

a second comparator which determines if the received link data contains a second IDLE sequence of said IDLE signal;

said Jabber counter which counts each cycle of a link clock in which an IDLE signal is not detected, and resets said count each time said IDLE signal is detected, and which asserts a DISABLE signal for a single link clock cycle if said count reaches said programmed time-out value; and

a logic gate which logically combines outputs from said first and second comparators and said Jabber counter to generate a Write control signal for prohibiting a corresponding link data sequence from being stored in said memory storage so as to prevent data overflow in said memory storage.

20. (Original) The computer network as claimed in claim 19, wherein said Jabber counter comprises:

a N-bit counter which counts each cycle of said link clock in which an IDLE signal is not detected, and resets said count each time said IDLE signal is detected and said DISABLE signal is asserted for a single link clock cycle if said count reaches said programmed time-out value;

an OR gate which logically combines outputs from said first and second comparators and said DISABLE signal to reset said count of said N-bit counter; and

a N-bit equality comparator which compares said count of said N-bit counter with said programmed time-out value and asserts said DISABLE signal if said count reaches said programmed time-out value.

21. (Original) The computer network as claimed in claim 17, wherein said memory storage corresponds to one of a first-in first-out (FIFO) register and a succession of D-type flip-flops having an elasticity required to synchronize said link data to said receiver clock.

22. (Original) The computer network as claimed in claim 17, wherein said link data is received via said physical links in compliance with the Next Generation I/O (NGIO) Link Architecture Specification.

23. (Original) The computer network as claimed in claim 17, wherein said plurality of addressable memory locations of said memory storage are determined by the difference in frequency of the link clock and the receiver clock, and non-IDLE characters included in said link data.

24. (Original) The computer network as claimed in claim 17, wherein said read control mechanism comprises:

a read pointer which operates at said receiver clock for selecting as said read address the address of a memory location of said memory storage to retrieve said link

data as said receiver data in dependence upon whether said memory storage is determined empty;

an output controller which determines said memory storage as empty when said read address corresponds to said write address; and

an output selector which inserts said No-Operation (NOP) sequences into said receiver data when said memory storage is determined empty.

25. (Original) The computer network as claimed in claim 17, further comprising a synchronizer which synchronizes the current value of said write address in a link clock domain with the current value of said read address in a receiver clock domain.

26. (Original) The computer network as claimed in claim 17, wherein said write pointer comprises a gray code counter.

27. (Original) The computer network as claimed in claim 24, wherein said output controller comprises:

a plurality of XNOR gates each of which logically combines said read address and said write address in synchronous with said read address; and

an AND gate which logically combines logic outputs from the XNOR gates and produces an output signal indicating whether said memory storage is empty.

28. (Original) The computer network as claimed in claim 24, wherein said read pointer comprises a gray code counter.

29. (Original) The computer network as claimed in claim 24, wherein said output selector comprises a multiplexer for selecting between said receiver data and said NOP sequences inserted in said receiver data in dependence upon whether said memory storage is determined empty.

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

Please cancel claims 5, 6, 18, and 30-35 without prejudice to or disclaimer of the subject matter contained therein.